1. (Previously Presented) A computer-implemented method for identifying the best process path in a semiconductor manufacturing process for processing a plurality of wafer lots, comprising:

providing a plurality of operation in the semiconductor manufacturing process;

providing a plurality of tools in at least one of the plurality of operations;

providing a plurality of process paths;

providing a plurality of lot yields corresponding to the plurality of wafer lots;

setting the plurality of lot yields as responses;

setting the plurality of operations as control factors;

setting the plurality of tools as factor levels in response to at least one of the plurality of operations;

determining at least one of the plurality of operations by using an analysis of variance method with the responses, control factors, and factor levels;

determining a best tool for the one of the plurality of operations having the most influence by retrieving a maximum statistical characteristic; and

outputting at least one best process path from the plurality of process paths, wherein the at least one best process path includes the best tool.

2. (Previously Presented) The method as claimed in claim 1, wherein the statistical characteristic comprises a signal to noise ratio.

3. (Previously Presented)) The method as claimed in claim 1, wherein the statistical characteristic comprises an average yield.

4. (Previously Presented) The method as claimed in claim 3, further comprising determining at least one of the plurality of tools corresponding to the at least one of the plurality of operations as having the most contribution to the average yield.

5. (Previously Presented) The method as claimed in claim 3, wherein the step of determining at least one of the plurality of operations by using an analysis of variance method includes,

comparing each of the plurality of operations relative to the average yield,

ignoring the plurality of operations having only a single tool, and

considering the plurality of operations having a greater than a predetermined level of contribution over the average yield.

6. (Previously Presented) The method as claimed in claim 1, wherein the best process path includes the tool having the most contribution.

7. (Previously Presented) A computer-readable medium storing instructions executable by a processor for identifying the best process path in a semiconductor manufacturing process for processing a plurality of wafer lots, comprising:

providing a plurality of operations in the semiconductor manufacturing process;

providing a plurality of tools in at least one of the plurality of operations;

providing a plurality of process paths;

providing a plurality of lot yields corresponding to the plurality of wafer lots;

setting the plurality of lot yields as responses;

setting the plurality of operations as control factors;

setting the plurality of tools as factor levels in response to at least one of the plurality of operations;

determining at least one of the plurality of operations by using an analysis of variance method with the responses, control factors, and factor levels;

determining a best tool for the one of the plurality of operations having the most influence by retrieving a maximum statistical characteristic; and

outputting at least one best process path from the plurality of process paths, wherein the at least one best process path includes the best tool.

8. (Previously Presented) The computer-readable medium as claimed in claim 7, wherein the statistical characteristic comprises a signal to noise ratio.

9. (Previously Presented) The computer-readable medium as claimed in claim 7, wherein the statistical characteristic comprises an average yield.

10. (Previously Presented) The computer-readable medium as claimed in claim 9, further comprising determining at least one of the plurality of tools corresponding to the at least one of the plurality of operations as having the most contribution to the average yield.

11. (Previously Presented) The computer-readable medium as claimed in claim 9, wherein the step of determining at least one of the plurality of operations by using an analysis of variance method includes,

comparing each of the plurality of operations relative to the average yield,

ignoring the plurality of operations having only a single tool; and

considering the plurality of operations having a greater than a predetermined level of contribution over the average yield.

12. (Previously Presented) A computer-implemented method for identifying the best process path in a semiconductor manufacturing process, comprising:

providing a plurality of operations in the semiconductor manufacturing process;

providing a plurality of tools in at least one of the plurality of operations;

providing a plurality of process paths;

providing a plurality of lot yields corresponding to the plurality of wafer lots;

setting the plurality of lot yields as responses;

setting the plurality of operations as control factors;

setting the plurality of tools as factor levels in response to at least one of the plurality of operations;

determining at least one of the plurality of operations by using an analysis of variance method with the responses, control factors, and factor levels;

determining a best tool for the one of the plurality of operations having the most influence by retrieving a maximum statistical characteristic; and

outputting at least one best process path from the plurality of process paths, wherein the at least one best process path includes the best tool.

13. (Previously Presented) The method as claimed in claim 12, wherein the statistical characteristics is a signal to noise ratio of the plurality of wafer yields.

14. (Previously Presented) The method as claimed in claim 12, wherein the best process path of the semiconductor process includes the tool having the most contribution.

Claims 15-17 (cancelled).